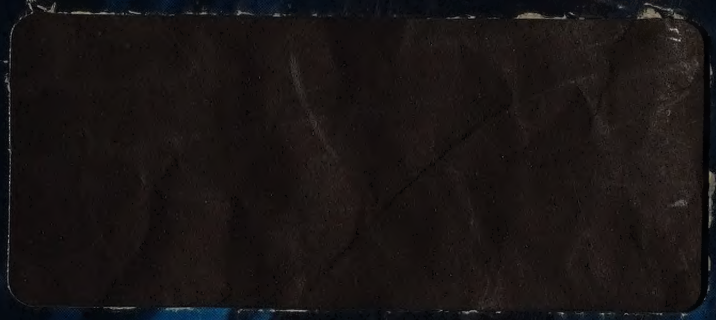
LeCroy



instrumentation
for the study of
transient phenomena

PALO ALTO, CA.

technical information manual

CAMAC Model 8258
High-Speed 20 MHz Video Digitizer

WARRANTY

All LRS instruments are guaranteed to operate within their specifications for one year from the date of purchase. Under this warranty, any unit which fails to perform within specifications, as a result of defects in workmanship or materials, will be restored to specified operating condition free of charge except for shipping costs involved in the return of the unit to the factory.

In order that this warranty be considered valid, it is necessary that the LRS Warranty Card which accompanies the unit on delivery be completed and returned to the factory within 30 days of receipt of equipment.

All questions concerning repairs or replacement parts should be addressed directly to factory's Quality Control Manager. This procedure will insure the fastest possible service. Please include the Model Type, Serial Number, and ECN (Engineering Change Number) with all requests for parts or service.

ENGINEERING DEPARTMENT
LeCroy / CALIFORNIA
PALO ALTO, CALIFORNIA

OCTOBER 1979

N O T I C E N O T I C E N O T I C E N O T I C E

Model 8258 with serial number 47933 has been modified as requested by ARGO Systems.

1.) "SYNC" Bit Logic is not active.

2.) Front Panel "SYNC" input has been replaced with "Stop Trigger".

3.) Unit will go into the read mode in normal fashion or can be stopped with high "TTL" signal at the "Stop Trigger" input on the front panel before memory is filled.

NOTE:

Circuit changes are annotated on schematics. Red markings indicate additions and/or changes. Yellow markings indicate components deleted and connections removed.

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7. Standard LeCroy Drafting Instructions

CAMAC Model 8258

VIDEO DIGITIZER

LED indicates the 8258 is ready to digitize

LED indicates the 8258 is digitizing

Offset measurable in millivols at TEST POINT

TTL pulse into 50Ω sets 9th bit of sample being digitized

Arms the unit to permit sampling upon receipt of clock pulse

TTL edge causes a sample to be taken and digitzed, 50Ω, minimum average frequency, 512 KHz, max. 20 MHz

LED indicates that the data is ready to be read

Push button sets 8258 to ready mode

10 turn pot to vary the offset from -256 mV to +256 mV

50Ω input impedance, full scale range 512 mV

Enables output of data via external fast port. TTL - 50Ω

TTL pulse whenever the last memory word is accessed (read or write)

ENGINEERING DEPARTMENT
LeCroy / CALIFORNIA
PALO ALTO, CALIFORNIA

TECHNICAL DATA

LeCroy
CALIFORNIA

CAMAC Model 8258

High-Speed 20 MHz Video Digitizer

- **High-speed digitizing**—1075 samples/line
- **Mass memory compatible**—4-way digital multiplexing
- **Fast parallel external port**—8 MHz maximum
- **Easy computer readout**—CAMAC interfacing
- **Memory expandability**—up to 64 32K memory modules
- **Unique CCD Compatibility**—20 nsec acquisition time
- **Standard TV compatibility**—synchronization bit

LeCroy Research Systems of California has developed a high-speed (20 MHz) mass memory (128 K) waveform digitizer particularly suited for digitizing the output of a vidicon or solid state (CCD) television camera. The minimum memory allows storage of half of a full 512 by 512 television matrix. Memory expandability can accommodate up to 8 full-size TV frames.

The performance of the digitizer does not compromise the analog recording capabilities of vidicon or CCD imagers in any way. A high-speed external data port permits DMA transfers up to 8 MHz/word rates. Standard CAMAC packaging simplifies computer interfacing and standardizes computer programming necessary to extract the data.

This digitizer is useful for applications with high E & M backgrounds, image intensifiers, streak camera digitization, and pinex cameras, where large amounts of data need to be acquired and stored at a high rate. CAMAC packaging results in a very economical system.

April 1979

Instrumentation for the study of transient phenomena

LeCROY RESEARCH SYSTEMS OF CALIFORNIA • 1806 Embarcadero Rd. • Palo Alto, California 94303
TELEPHONE: (415) 856-1800 TWX: 910-373-1791

SPECIFICATIONS
CAMAC Model 8258
High-Speed 20 MHz Video Digitizer

Input Characteristics

Signal Range: 512 mV full scale into a 50 (75)Ω impedance.

DC Offset Adjustment: −256 mV to +256 mV. Front-panel potentiometer permits adjustment of blanking level or accommodates either positive- or negative-going video input.

Amplifier Noise: 50 μV.

Analog Bandwidth: Full-scale sine wave: 3 dB point = 30 MHz. (Horizontal resolution = 4586 TV lines.) 20% F.S. sine wave: 3 dB point = 70 MHz.

Risetime: 15 nsec, 10–90%.

Track and Hold Acquisition Time: 20 nsec to ½% accuracy.

Connectors: LEMO-type.

Overvoltage Protection: Protected against ±5 A transients for 0.5 μsec, clamping at ±1 V.

Track and Hold Sampling Jitter: ±25 psec.

Overload Recovery: 500 nsec for voltage 5 times full scale less than ½ μsec long.

Sampling Control and Digitization

External Sampling Strobe: TTL levels. Permissible strobe rate 500 MHz to 20 MHz. Use of LeCroy/California dynamic RAM memory requires a minimum frequency of 500 KHz. 50Ω impedance. LEMO-type connector. Minimum duration 20 nsec.

Synchronization Input: TTL level sets a ninth digital bit to the true state to be stored with the digitized signal for the duration of the input. Information is used typically to flag words digitized during "flyback" of the readout electron beam, but can be used as a general timing flag.

Digital Resolution: 1 part in 256 (8 bits) corresponding to 2 mV/count.

Throughput Rate: 20 MHz maximum. This rate corresponds to 1075 samples/line.

DC Linearity: ±0.4% deviation from the best straight line.

General System Performance

Harmonic Distortion: The Integrated Power Spectrum over all frequencies generated by the digitizer in response to a single pure sine wave (input frequency excluded from the sum) relative to the input power.

Analog Input Frequency	0–5 MHz	5–8 MHz	8–10 MHz
Harmonic Distortion	48 dB (1/256)	42 dB (1/128)	36 dB (1/64)

Memory and Readout

Memory: A minimum of four LeCroy/California 8800/9 32K-word 9-bit memory modules are necessary to store data from the digitizer at 20 MHz. At 10 MHz and 5 MHz maximum rates, the minimum required memory sizes are 2-8800/9 and 1-8800/9 respectively (jumper option). Further expansion of the memory is possible in 2, 3 or 4 module steps to a total of 64 memory modules. (See the 8800 series data sheet for specs and power requirements.) Model 8800/8 memory can also be used when synchronization information is not needed.

Memory Control: The digitizer control board multiplexes the data to four separate digital output ports. The number of memory modules per output port must be reflected in the memory switch settings.

Module Interconnections: Four 40-conductor flat cables, one per digital output port. LeCroy Model DC8800/n cables are expressly constructed to provide this connection where n refers to the number of memory modules per branch.

CAMAC Commands: X: An X = 1 (Command Accepted) response is generated when a valid F or N command is generated.
Q: A Q = 1 response is generated in recognition of an F(2) for a valid N, if data is present, or in recognition of an F(8), if the LAM is set. After the last word has been read from memory, the next read will generate a Q = 0 response.
L: A Look-At-Me is generated at the end of the sampling sequence, if previously enabled by F(26).

Function Codes: F(0): Read pedestal.
F(2): Read data register; requires N. (Two 8-bit samples plus two sync bits are packed into one data record in the following way:

Sample 1: R1–R8 Sync bit 1: R17
Sample 2: R9–R16 Sync bit 2: R18

Successive F(2)·N commands read successive 18-bit words from the memory. If the pattern select mode is enabled by an F(25) command, the 9-bit data byte will be transformed into an 8-bit data byte according to the following algorithm:

Bits (0–7)	Bit (8)		Results
XXXXXXXX	0	=	XXXXXXXX
XXXXXXXX	1	=	00000000
00000000	0	=	00000001
00000000	1	=	00000000

Successive F(2)·N commands read successive 18-bit words from the memory. If the pattern select mode is enabled by an F(16) command, the 9-bit data byte will be transformed into an 8-bit data byte according to the following algorithm:

F(10): Clear LAM.
F(16): Enable pattern select data mode.
F(24): Disable LAM.
F(26): Enable LAM; Enable CAMAC readout.

External Data Port: Front-panel input (TTL level for 100 nsec) initiates sequential transfer of 9-bit words of parallel data from memory. Transfer continues until all memory has been read at an adjustable rate between 500 KHz and 8 MHz.

Packaging: Standard CAMAC packaging for nuclear modules (USAEC Report #TID-25875, European Esone Report #EUR 4100e, IEEE Standard #583). RF-shielded #3 width CAMAC module. Minimum system width with 4 memory modules: 7 CAMAC widths.

Approximate Power Requirements:

	+6 V	−6 V	+12 V	+24 V	−24 V
8258 Video Digitizer	3 A	3.5 A	0 A	0.2 A	0.2 A
8800 memory Block (4 modules)	2.6 A	0.120 A	1.3 A*	0 A	0 A

*Derived from +24 V if +12 V not available.

3. ADDENDA TO SPECIFICATIONS

1. DMA transfers up to 8 MHz/word rates

2. External sampling strobe: permissible rate 512 KHz - 20 MHz

3. Throughput rate: 20 MHz maximum - 512 KHz minimum

4. L: A Look-At-Me is generated after the first data word's ready to be read, previously enabled by F(26).

5. F(0): Read pedestal

6. F(2): Read data register, requires N. (Two 8-bit samples plus two sync bits are packed into one data record in the following way:

Sample 1: R1 ÷ R8 Sync bit 1: R17
Sample 2: R9 - R16 Sync bit 2: R18

Successive F(2)·N commands read successive 18-bit words from the memory. If the pattern select mode is enabled by an F(16) command, the 9-bit data byte will be transformed into an 8-bit data byte according to the following algorithm:

Bits (0-7)	Bit (8)		Results	Bits (0-7)
XXXXXXXX	0	=	XXXXXXXX	
XXXXXXXX	1	=	00000000	
00000000	0	=	10000000	

7. F(16): Enable pattern select

8. External Data Port: Adjustable transfer rate between 512 KHz and 8 MHz

9. Deletions: Z or C: Clears all registers

F(11): Disable pattern select data mode

10. The "ENABLING" input must be set to a TTL HI state during the entire SAMPLING period. After the 8258 module enters the READ mode, the "ENABLING" input must be set to a TTL LO state.

4. OPERATIONAL DESCRIPTION

4a. General

The LRS Model 8258 Waveform Digitizer is an eight bit analog to digital converter with 128K of memory. The amount of memory is expandable to 2048K and the unit can sample and digitize a waveform at any rate between 512 KHz and 20 MHz. The A/D conversion is accomplished by performing two consecutive 4 bit flash comparisons. The first comparison yields the upper four bits (2^7 to 2^4). These bits are then reconverted to an analog signal which is subtracted from the original input analog signal. The remaining signal is then put through the second flash converter to give the least significant bits (2^3 -2^0).

The Model 8258 can be in one of three states or modes. The front panel LED's indicate the state of the system. When the 8258 is in the READY mode, it is ready to digitize the analog input signal. Once digitizing starts, the unit is in the SAMPLING mode. After the memory is filled with data, the 8258 enters the READ mode. In the READ mode, data can be read from memory using a CAMAC dataway or the fast port.

In order to read data via the CAMAC dataway, a F(26) cycle must be executed. This command sets a flip-flop in the controller called the CAMAC Read Enable (CREN) flip-flop. If this flip-flop is set, the data in memory can be read using F(2) commands.

A second flip-flop called the Fast Port Enable flip-flop can be set using the front panel controls. Data can be output to the fast port only when this flip-flop is set.

4b. FRONT PANEL CONTROLS AND INDICATORS

Analog Input: The analog input has a 50 Ω impedance and an amplitude range of 512 mV. A front panel D.C. offset potentiometer permits adjustments of up to ±256 mV (±20 mV) providing an operational usefulness for positive unipolar through bi-polar to negative unipolar pulses. The offset measurement is available for computer readout. Table 1 gives a list of input voltages vs. binary output codes for various D.C. offsets. The fullscale 3 dB bandwidth of the linear input circuitry is 30 MHz. For signals 20% of fullscale the bandwidth is 70 Mhz.

~~INITIATE~~ RESET: The INITIATE button on the front panel will set the 8258 into the READY mode.

4c. CAMAC CONTROL

L: A Look-At-Me signal is generated after the first data word is ready to be read.

Q: A Q=1 response is generated in recognition of F(2) · N when a valid word is being read.

A Q=1 response is generated in recognition of F(8) · N if LAM is set. If LAM is not set, Q=0 is generated.

X: An X=1 response is generated when a valid F and N are detected.

F(0): The data on R1-R8 is equal to the pedestal.

F(2): Read 2 words of data. R1-R8 equals the first data word (R1=LSB), R9-R16 equals the second word. (R9=LSB). R17 equals the sync bit associated with the first word. R18 equals the sync bit associated with the second word. Requires N.

F(8): Test LAM. Requires N. Q response is generated to indicate LAM status.

F(10): Reset LAM. Requires N.

F(9): Same as depressing front panel INITIATE switch. Clears LAM and LAM enable. Requires N.

F(16): Enable pattern select. When data is accessed from memory, if F(16) was executed, the 9-bit data bytes are transformed using the following hardware algorithm.

Bit 7	Bit 0	Sync.	TRANSFORMED DATA
xxxxxx	x	1	00000000
xxxxxx	1	0	xxxxxxx1
000000	0	0	00000001

Each time the last word in memory is read, the pattern select function is disabled.

Requires N.

F(24): Disable LAM. Disable CAMAC Read Enable Flip-Flop.

F(26): Enable LAM. Enable CAMAC Read. Enable flip-flop (CREN). LAM is reset by F(9).

ENABLING:	This input expects a TTL level. If this input is HI, and the unit is in the READY mode, each positive (LO→HI) clock transition at the clock input initiates an A/D conversion.
CLOCK:	This input has a 50Ω impedance and expects TTL levels. The frequency of the clock is variable between 512 KHz and 20 MHz. The positive edge of the signal initiates conversions if the ENABLE signal is at a TTL HI level. Once sampling begins, it must continue until L.M.W. is generated or else all data will be lost. It is recommended that this clock run continuously. Digitizing should be controlled using the "Enabling Sampling" input.
SYNC:	This input has a 50Ω impedance and expects TTL levels. The level present at this input at each positive clock transition is written into memory as a 9th bit, along with the A/D output initiated by an edge two clock pulses before the current positive clock transition.
ARM EXTERNAL:	This input has a 50Ω impedance and expects TTL levels. The first positive transition (LO→HI) at this input after the module is in the READ mode, enables the fast port. A clock must be supplied by the user to output data to the fast port. (See FAST PORT MODE, Section 4d).
L.M.W.	After the last memory location in the system is accessed (either by a read or write operation), a 1μsec. TTL level pulse is generated.
READY LED:	A lighted LED indicates the Model 8258 is ready to digitize. The first positive clock transition after the ENABLE input is set HI will initiate conversions.
SAMPLING LED:	This LED is lighted when the unit is digitizing the analog input signal.
READ LED:	The module automatically enters the READ mode and lights this LED after the last sample is digitized and the memory is filled.

After a F(26) is executed, the LAM will be set when the first data word is ready to read. If the CREN flip-flop is turned on while data is being output to the fast port, (i.e. Fast Port Enable is set), the LAM will be set after the last word in memory is output to the fast port. At this point F(2) commands will read valid data and each F(2) cycle will generate a Q=1 response.

CREN is automatically reset after the last word in memory is read using the F(2) command.

4d. FAST PORT MODE

The data in memory can be output one word at a time (8 data bits + 1 sync. bit) to a 40 pin connector at the rear of the module. The user must supply a clock signal with a frequency between 512KHz and 8MHz. The clock signal is input through the same rear connector, over which the data is transferred.

In order to use the fast port, a transition from a TTL low level to a TTL hi level must be supplied at the Port Enable input at the front panel. This transition sets the Fast Port Enable flip-flop. Once this flip-flop is set, the fast port clock (this is not the same as the front panel clock) must run continuously until all the data in memory is read. For this reason, it is suggested that the fast port clock always be left on.

The Model 8258 ignores the fast port clock unless the Fast Port Enable flip-flop is set. All transitions at the Port Enable input are also ignored if the Model 8258 is not in the READ mode or the CREN flip-flop is set.

MECHANICAL: Uses a 40 conductor flat cable. Connector-mate to spectrastrip #802-040 or equivalent.

PIN OUT:

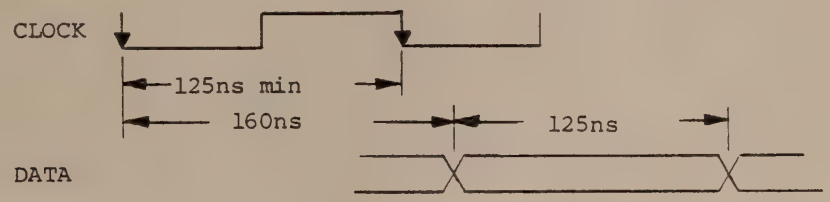
PIN #	SIGNAL
17	Data Bit ϕ (LSB)
15	1
13	2
11	3
9	4
7	5
5	6
3	7
1	Sync.
19	Clock

Pins 2, 4,...,40 are ground.

ELECTRICAL: CLOCK - TERMINATED in 100Ω.

DATA and SYNC BITS: TTL 50-Ω LINE DRIVERS (74128)

TIMING:



5. FUNCTIONAL DESCRIPTION

5a. CONTROLLER

The controller contains two sets of buffers. Each set consists of four one-word buffers. One set is used when writing data into the memories and one set for reading from memory.

After a conversion, the ADC output is transferred to a write buffer. When all four buffers are filled, the data in the buffers are transferred to four memory modules.

This sequence continues until the memory is filled. At this point, one of the memory modules sends a "L.M.W." signal to the controller and no more data is transferred from the buffers. The "L.M.W." signal also forces the module into the read mode and fills the four read buffers with the first four words, which were written into memory.

In the fast port read mode, each positive clock transition input by the user at the fast port transfers data from one read buffer to the port. After four clock pules, the buffers (which are now empty) are immediately filled again with data from memory.

A similar sequence of events occurs if an F(26) is detected. Data from the buffers passes into a set of F1F0's and can be read using F(2) commands.

5b. ADC Section

1. General Description: The analog to digital converter in the Model 2256 is a two stage parallel-serial type converter. The four most significant bits (MSB's) are obtained from a flash converter consisting of 15 high speed comparators whose outputs are reduced to binary form by a fast encoder. The binary (MSB) outputs are then fed into an output latch and into the inputs of a high speed 4 bit DAC. A signal proportional to the difference between the DAC output and the input signal is constructed by a fast difference amplifier. This difference signal is then digitized by another 4 bit flash converter. The encoded outputs of the second converter are the least significant bits (LSB's) of the ADC and they are also latched for transfer to memory.

In front of the ADC is a fast track and hold circuit with a well defined aperature time (aperature jitter ±25 psec) which presents fixed voltage samples of the ADC for digitization eliminating slewing problems in the comparators.

Preceding the track and hold is a fast X10 amplifier (VV100) whose output can be offset over a range of 5.12 volts, the input range of the ADC, to allow optimum use of the ADC range for various types of signals. The signal inputs to the Model VV100 must lie in a 512 mV interval determined by the DC offset voltage (see Table I). The input to the Model VV100 is disconnected from the input signal after the last sample is taken to measure the combined effects of ADC pedestal and offset voltage.

2. Detailed Description:

VV100 Input Amplifier - A LeCroy hybrid 300 MHz amplifier with appropriate external circuitry to allow for adjustment of the output offset between -2.56 V and +2.56 V. The bandwidth of the amplifier has also been reduced to 70 MHz by a compensation network to provide stable operation in this circuit configuration.

Track and Hold Circuit - The track-and-hold circuit consists of a balanced diode sampling gate which is switched by a fast comparator in conjunction with a differential pair providing proper voltage and current inputs to the diode bridge switch. The output of the gate is connected to a unity gain high speed discrete amplifier, which is basically a differential cascade amplifier with a complimentary symmetry push-pull output. When the gate is open the amplifier tracks the input signal and the instantaneous output voltage is imposed on a small hold capacitor. When the gate is closed, the signal is held at the level stored on the capacitor. Input bias current is provided by a pair of thermally compensating PNP transistors which also compensate for capacitor leakage.

In operation the circuit tracks for about 20 nsec during which time it is able to acquire a full scale voltage change. The hold time is 30 nsec. About 20 nsec of that time is allowed for switching transients to decay and for the output voltage to settle to within a 1/2 LSB of its final value. The output of the track and hold is connected directly to the input of the first comparator chain. The 3 dB bandwidth for a full scale voltage change is 30 MHz.

ADC - The first 15 comparators have their switching levels set at 320 mV intervals between ±2.560 volts by a resistor chain and precision regulated bias voltages. As soon as the track and hold output has settled, the comparators are unlatched and allowed to swtich to states corresponding to their biasing and the signal level. The complementary outputs of the comparators feed a series of NOR gates whose outputs are wired ORed together. This gives a 4 bit binary output which is latched into the output register for later transfer to memory. The 4 bit binary signal is also applied to a DAC consisting of precision current sources and fast current switches. The DAC converts the 4 MSB's into an analog current which is applied to the summing node of a fast discrete op amp similar to the one used in the track and hold circuit. At the same time a current proportional to the input signal is applied to the summing node. This signal reaches the summing node through a delay line of sufficient length to allow for propagation and settling times. The input currents to the node are of such a polarity that the op amp output is proportional to the difference between the DAC output and the input signal. In order for this to be true over the entire input range, the DAC gain and offset must be precisely adjusted. The output of the subtractor op amp is then applied to another 4 bit flash converter like the one used to obtain the 4 MSH's but biased to fit the difference output voltage range of the subtractor. This second converter then yields the 4 LSB of the 8 bit output. The LSB's are latched into an output latch to be stored until transfer to memory occurs.

6. SYSTEM INTERCONNECTION___

a. The four flat cables extending from the rear of the 8258 are to be plugged into the four 8800/9 memory modules.

b. Be sure the dip switches in each 8800/9 (accessible through a cutout in the side panel) are in the following positions:

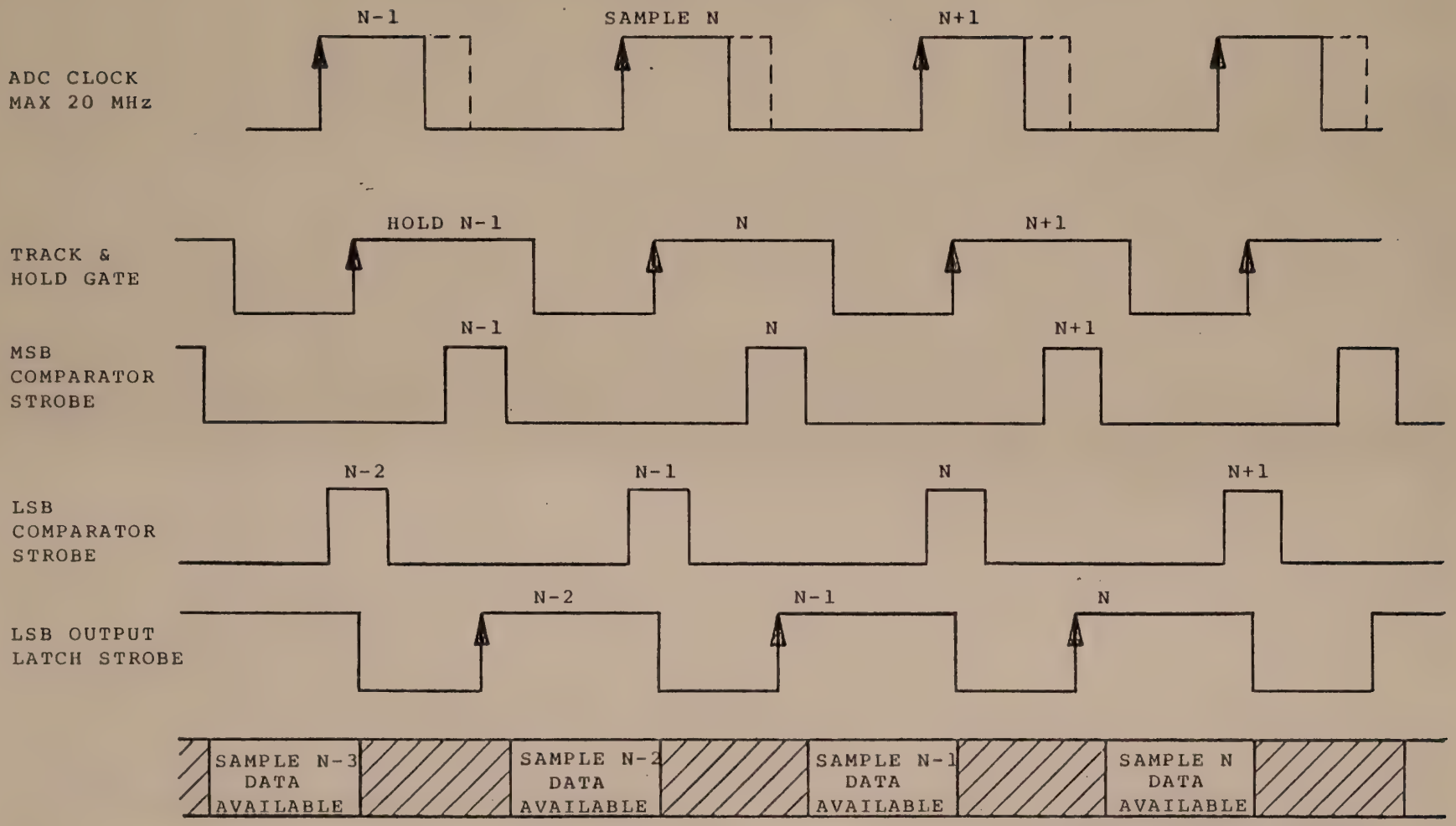
SWITCH	1	OFF
	2	ON
	3	ON
	4	OFF
	5	ON
	6	OFF
	7	OFF
	8	OFF

*FOR SYSTEMS USING MORE THAN FOUR MEMORY MODULES, SEE MEMORY MODULE TECHNICAL INFORMATION MANUAL FOR SWITCH POSITIONS.

TABLE I

Input Amplitude	DC Offset	Digitized DC Offset	Digitized Signal
-256 mV	0 mV	128	0
0 mV	0 mV	128	128
+256 mV	0 mV	128	256
-512 mV	+256 mV	0	0
-256 mV	+256 mV	0	128
0 mV	+256 mV	0	256
0 mV	-256 mV	256	0
+256 mV	-256 mV	256	128
+512 mV	-256 mV	256	256

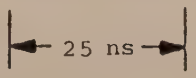
TYPICAL 8258 ADC TIMING



NOTE: 1) MSB DATA OUTPUT LATCHES ARE STROBED ON POSITIVE GOING EDGE OF TRACK & HOLD GATE (E.G. - SAMPLE N-2 MSB DATA IS LATCHED INTO OUTPUT LATCHES ON LEADING EDGE OF SAMPLE N-1 HOLD GATE).

2) DATA STROBED INTO MEMORY ON LEADING EDGES OF ADC CLOCK PULSES.

TIME SCALE



ECO NO.	DATE	PRIORITY	DESCRIPTION
1001	05-30-78		PC LAYOUT CHANGE. CORRECTIONS ON SCHEMATIC SHEETS 1-3. UPGRADED MATERIALS LIST.

Remarks: On Priorities
1-Recall, field retrofit
2-Rework shippable units
3-Rework units in fabrication, assembly or test
4-Improvements for future MO's

LeCroy RESEARCH SYSTEMS

DRAWN

CHECKED

DATE

ENGINEERING CHANGE ORDERS

MODEL: 8258

DRAWING NUMBER:

OGILVIE PRESS BUFFALO NY

ECO NO.	DATE	PRIORITY	DESCRIPTION
1000	-		NOT USED.
1001	-		NOT USED.
1002	12-8-78		CHANGED "R18" FROM 10K TO 1K. REPLACED IC "2C" WITH 74S112. REPLACED IC"1F" WITH 7411. CHANGED SCHEMATIC SHEETS 1-4. CHANGED "C13" FROM 100pf CERAMIC TO 100pf MICA (DM10). THE CHANGE FOR SIGNAL "CT" ON SHEETS 1 & 2 OF SCHEMATIC REQUIRED A PC CHANGE. CHANGED HOLE ON FRONT PANEL FOR 5K POT TO .182 D. CHANGED 100pf TO MICA.
1003	-		NOT USED
1004	03-14-79		PART DESCRIPTION STANDARDIZING. ADDED REVISION LEVEL OF PC ARTWORK TO PART #718-258-023.
1005	07-31-79		COMPONENT CHANGES TO ASSY DRWG., PARTS LIST, AND SCHEMATIC. ADD WIRE FROM 3H-11 to 1M-3 ON ASSY DRWG.
1006	1/8/80		PARTS LIST CHANGE: 510 OHM RES TO 620 OHM RESISTOR.

Remarks: On Priorities
1-Recall, field retrofit
2-Rework shippable units
3-Rework units in fabrication, assembly or test
4-Improvements for future MO's

LeCroy RESEARCH SYSTEMS

DRAWN

CHECKED

DATE

ENGINEERING CHANGE ORDERS

MODEL: 8258-2

DRAWING NUMBER:

OGILVIE PRESS BUFFALO NY

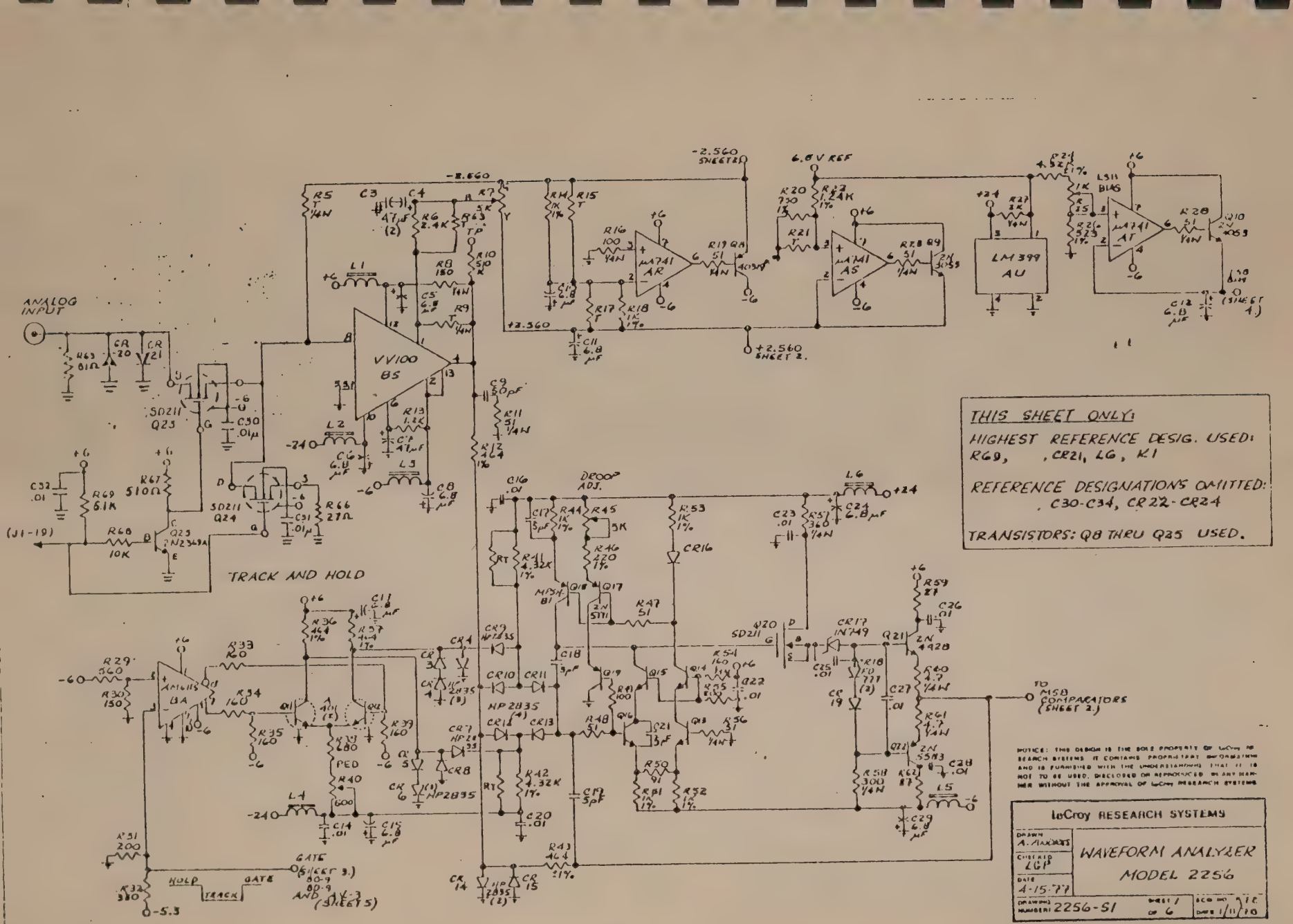
ECO NO.	DATE	PRIORITY	DESCRIPTION
1002	02-01-79		STANDARDIZATION OF HARDWARE. DELETED PART #'s 571-440-004, AND 571-440-006. ADDED: PART #560-440-004 AND 560-440-006.
1003	03-27-79		REV. LEVEL CHANGE IN ASSEMBLY

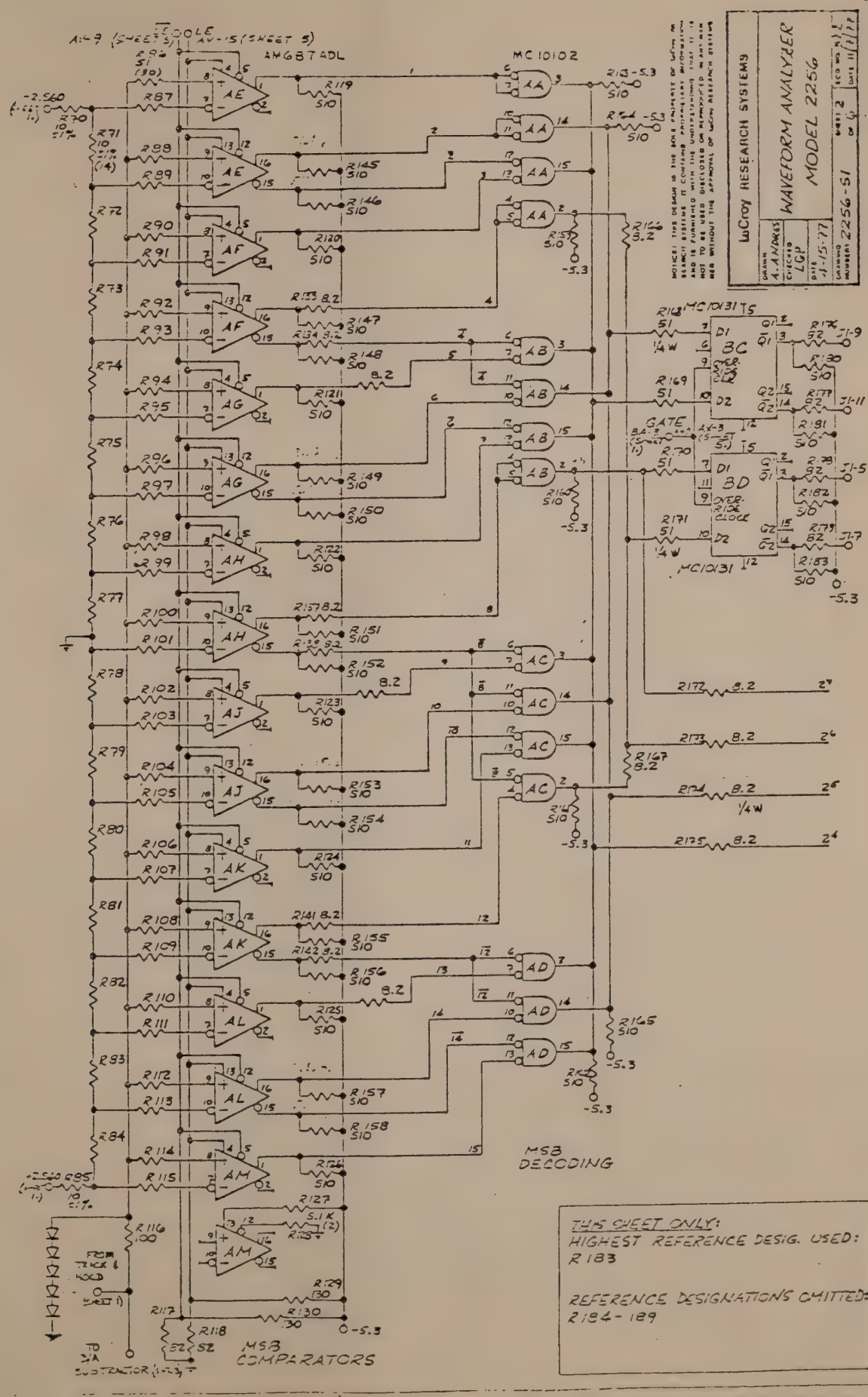
Remarks: On Priorities
1-Recall, field retrofit
2-Rework shippable units
3-Rework units in fabrication, assembly or test
4-Improvements for future MO's

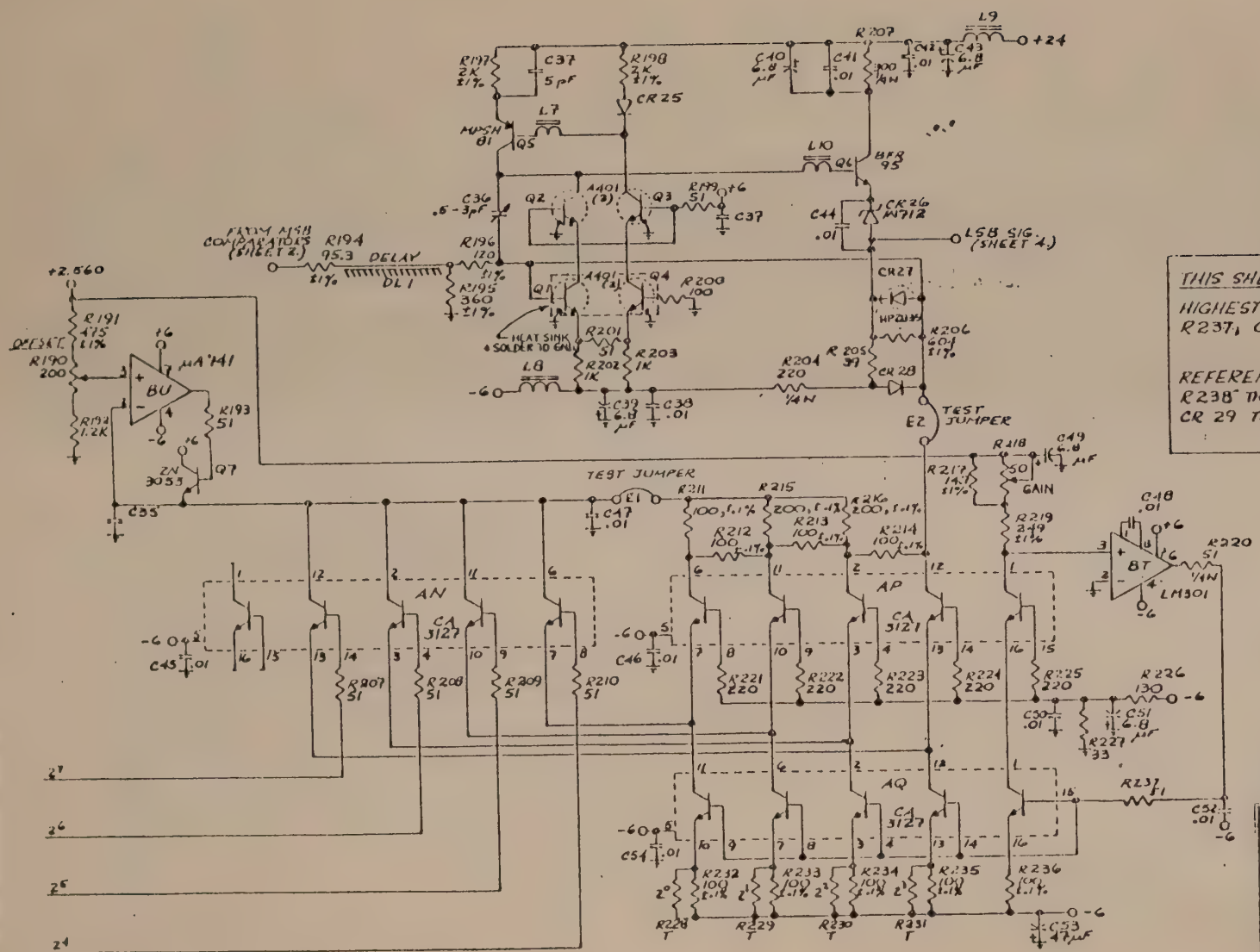
LeCroy RESEARCH SYSTEMS

DRAWN	
CHECKED	ENGINEERING CHANGE ORDERS
DATE	MODEL: 8258-3
DRAWING NUMBER:	

OGILVIE PRESS BUFFALO NY


ANALOG INPUT
TRACK AND HOLD
VV100 BS
MA741 AR
MA741 AS
MA741 AT
LM399 AU
-2.560 SHEET 2
+2.560 SHEET 2.
6.8 V REF
-2.560
+2.560
TO MISB COMPARATORS (SHEET 2.)
GATE (SHEET 3.) 80-9 AND 80-7 (SHEET 5)
HOLD
TRACK
GATE
THIS SHEET ONLY:
HIGHEST REFERENCE DESIG. USED: R69, , CR21, L6, K1
REFERENCE DESIGNATIONS OMITTED: , C30-C34, CR22-CR24
TRANSISTORS: Q8 THRU Q25 USED.
NOTICE: THIS DESIGN IS THE SOLE PROPERTY OF LeCroy RESEARCH SYSTEMS IT CONTAINS PROPRIETARY INFORMATION AND IS FURNISHED WITH THE UNDERSTANDING THAT IT IS NOT TO BE USED, DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE APPROVAL OF LeCroy RESEARCH SYSTEMS
LeCroy RESEARCH SYSTEMS
DRAWN A. MADDOCKS
CHECKED LGP
DATE 4-15-77
WAVEFORM ANALYZER MODEL 2256
DRAWING NUMBER 2256-51
SHEET 1 OF 6
ECO NO
DATE 1/11/78


LeCroy RESEARCH SYSTEMS
WAVEFORM ANALYZER
MODEL 2256
A. ANDRES
LGP
4/15/77
2256-51
AM687ADL
MC 10102
MC10131
GATE
MSB DECODING
MSB COMPARATORS
THIS SHEET ONLY:
HIGHEST REFERENCE DESIG. USED:
R183
REFERENCE DESIGNATIONS OMITTED:
R184-189



THIS SHEET ONLY:

HIGHEST REFERENCE DESIG. USED:
R237, C54, DL1, L10, CR28, Q7

REFERENCE DESIGNATIONS OMITTED:
R238 THRU 244, C55 THRU 59,
CR 29 THRU 34.

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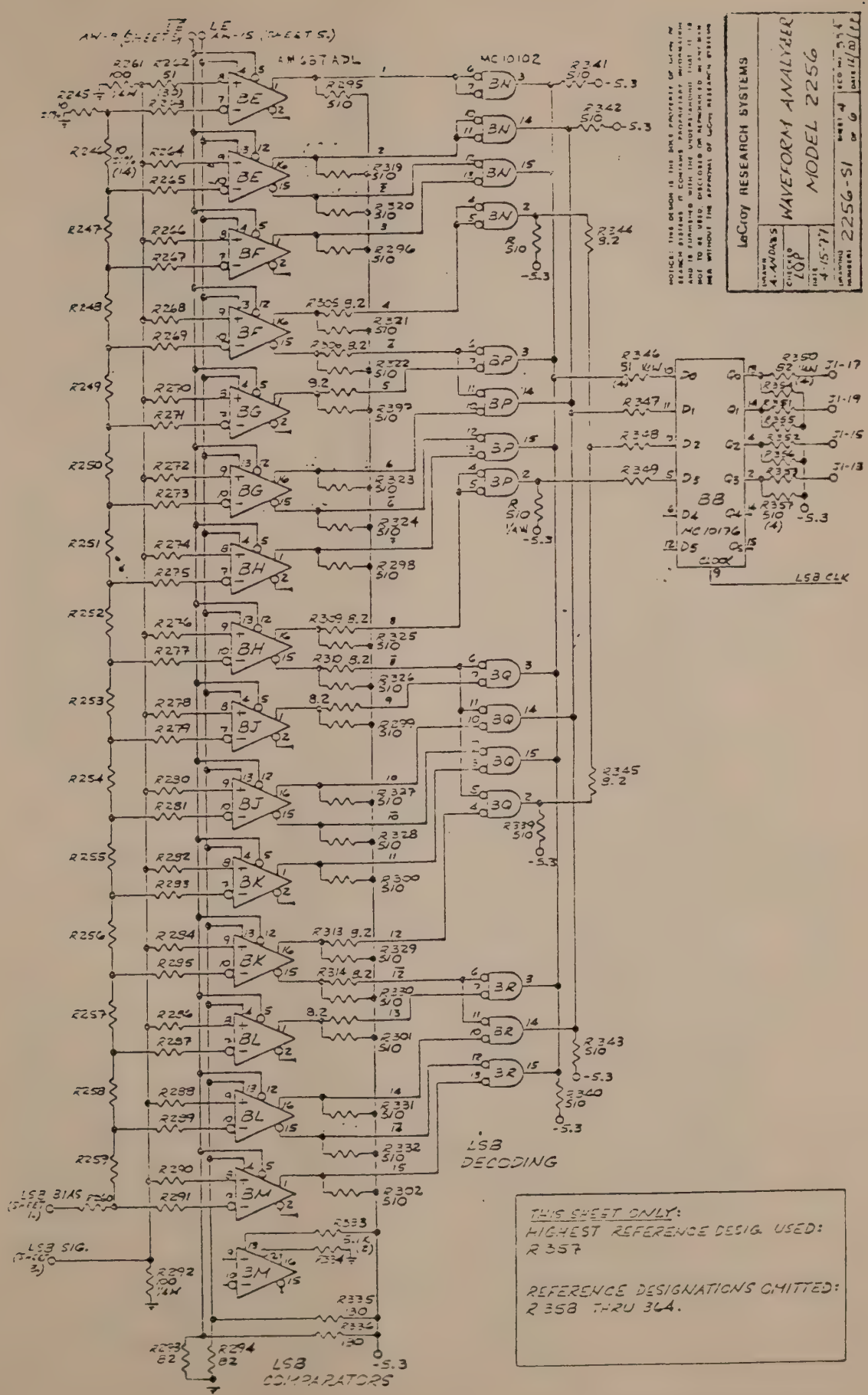
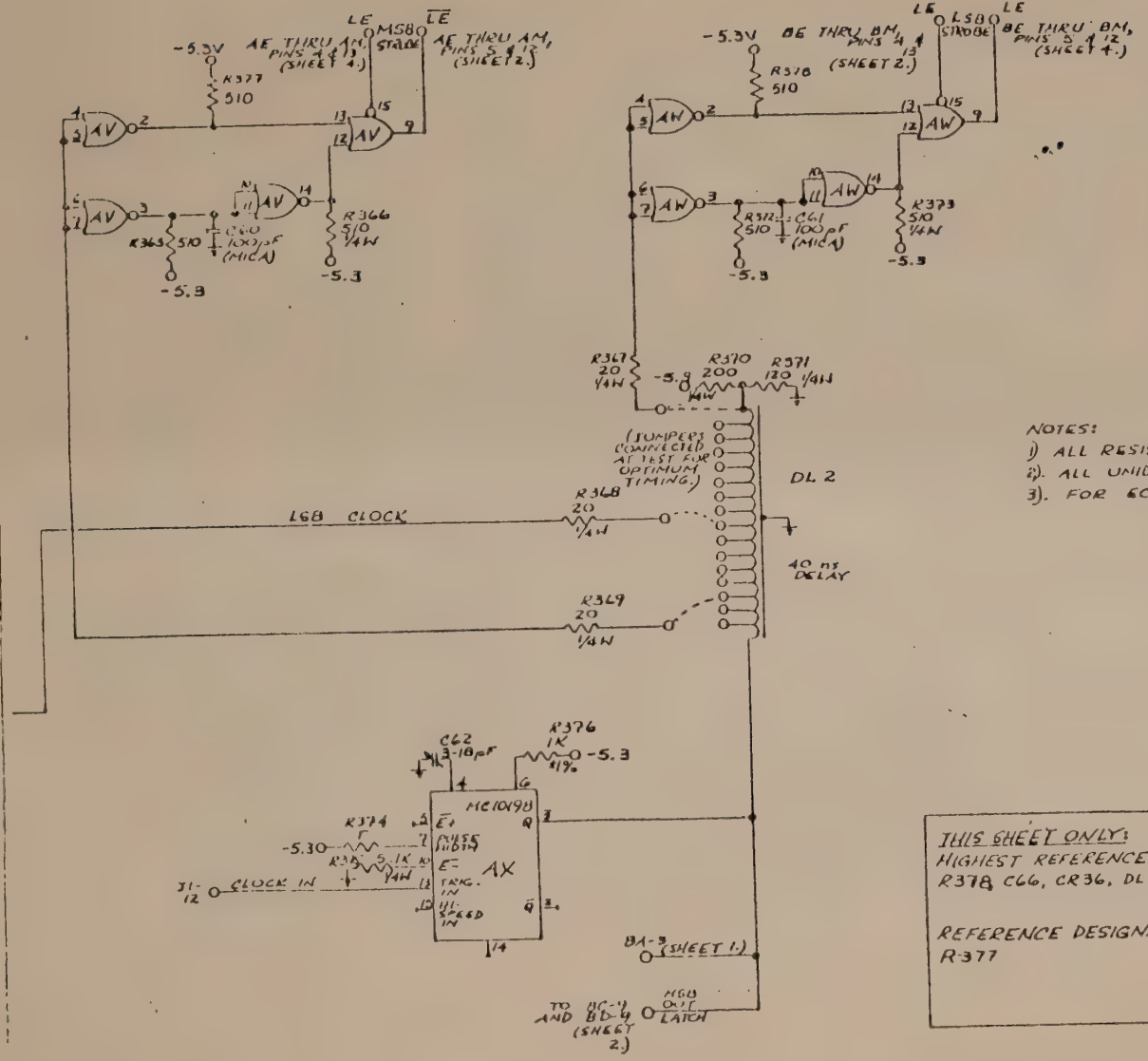
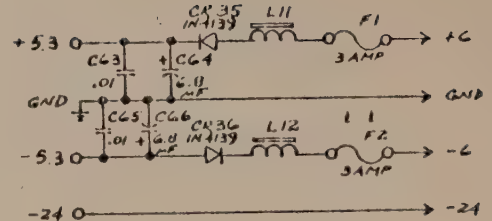
LeCroy RESEARCH SYSTEMS

DRAWN A. ANDRES	WAVEFORM ANALYZER MODEL 2256
CHECKED LGP	
DATE 1-15-77	
DRAWING NUMBER 2256-51	SHEET 3 OF 6
ECO NO. 574 DATE 12/2/77	


LeCroy RESEARCH SYSTEMS
WAVEFORM ANALYZER
MODEL 2256
2256-SI
4-15-77
LSB DECODING
LSB COMPARATORS
LSB CLK
LSB SIG.
LSB BIAS
THIS SHEET ONLY:
HIGHEST REFERENCE DESIG. USED:
R 357
REFERENCE DESIGNATIONS OMITTED:
R 358 THRU 364.





NOTES:
1). ALL RESISTORS ±5%, 1/8 W, UNLESS OTHERWISE INDICATED.
2). ALL UNIDENTIFIED DIODES ARE IN4448.
3). FOR ECL MEMORY AND CONTROL SECTIONS SEE 2256-92.

THIS SHEET ONLY:
HIGHEST REFERENCE DESIG. USED:
R378, C66, CR36, DL 2

REFERENCE DESIGNATIONS OMITTED:
R377

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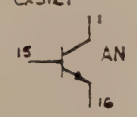
LeCroy RESEARCH SYSTEMS

DRAWN A. ANDRES	WAVEFORM ANALYZER MODEL 2256
CHECKED LGP	
DATE 4-15-77	
DRAWING NUMBER 2256-S1	SHEET 5 OF 6
ECO NO. 125 DATE 9/1/77	

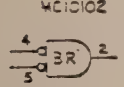
LRS PART #	I.C. #	DESIGNATIONS	+24 V	+6.0V	-5.3V	GND.	-5.3V	-6.0V
204 022 001	MC10198L	AX				1,16	8	
204 022 002	MC10176L	BB				1,16	8	
204 042 002	MC10102	AA,AB,AC,AD,AV,AW,BR,BP,BQ,BS				1,16	8	
204 042 005	MC10131P	BC,BD				1,16	8	
208 011 001	μA741C	AR,AS,AT,AU		7				4
208 011 003	LM301AN	BT		7				4
208 044 002	CA3127E	AN,AP,AQ	X	X	X	X	X	X
208 048 001	AM68T40DL	AE,AF,AG,AH,AI,AK,AL,AM, AE,BF,BG,BH,BI,BK,BL,BM			11	3,14	6	
208 068 001	AM685HL	BA		1		9,10		5
208 133 001	LM339H	AU	3			2,4		

UNUSED DEVICES:

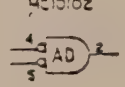
CA3127



MC10102



MC10102



NOTES:

1) "T" (IF ANY) DENOTES VALUE TO BE CHOSEN AT TEST.
2) UNIDENTIFIED DIODES ARE ALL IN4448.
3) POSSIBLE ADDITIONAL .01 μF AND 6.8 μF CAPACITORS, NOT SHOWN, ON VOLTAGE BUSES.
4) * DENOTES OPEN-COLLECTOR OUTPUT.
5) MATCHED TRANSISTORS: Q1 AND Q4 MATCHED AT 6V., 5 MA
   Q2 AND Q3 MATCHED AT 6V., 5 MA
   Q13 AND Q16 MATCHED AT 4V., 5 MA
   Q14 AND Q15 MATCHED AT 15V., 5 MA

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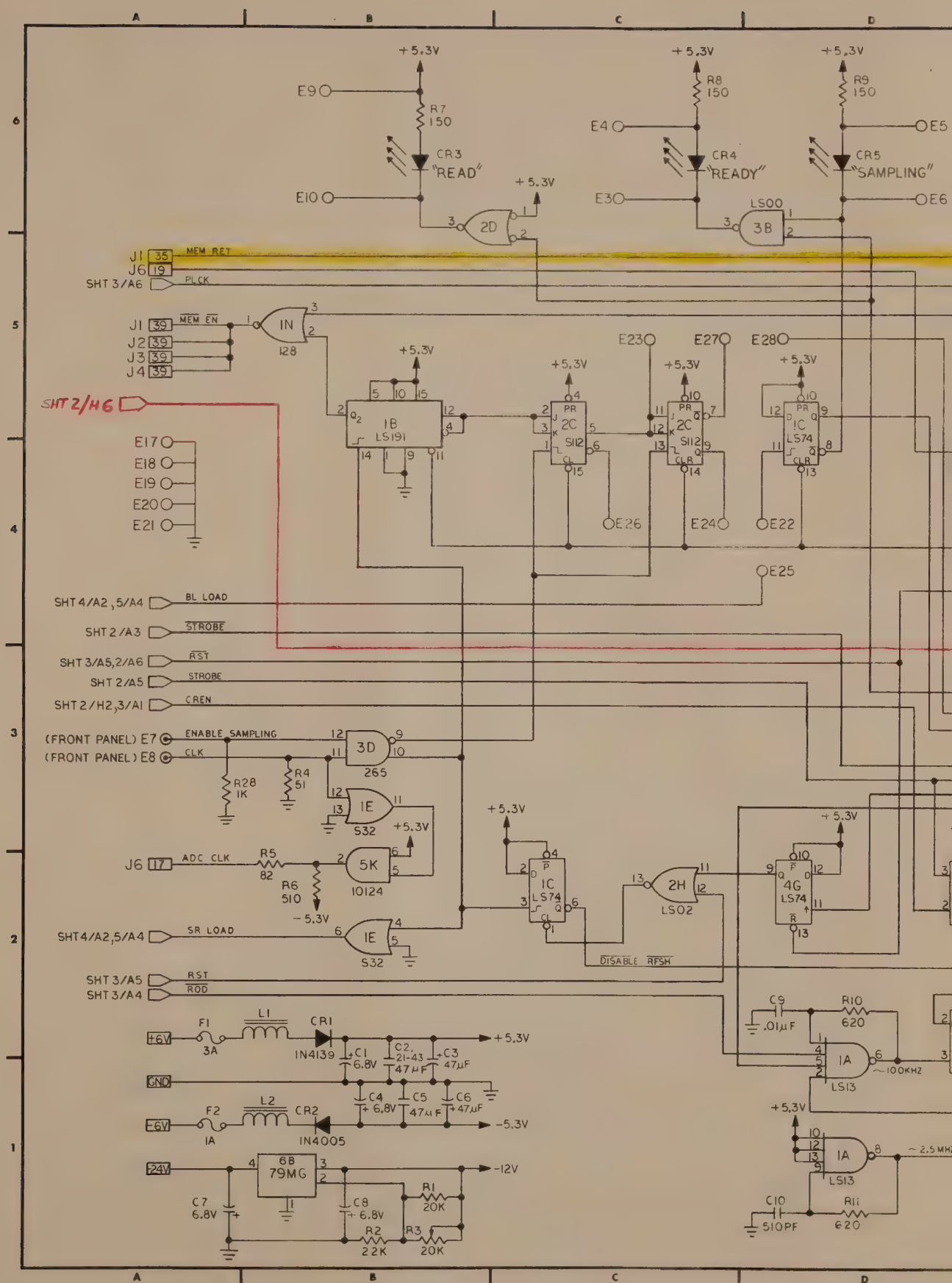
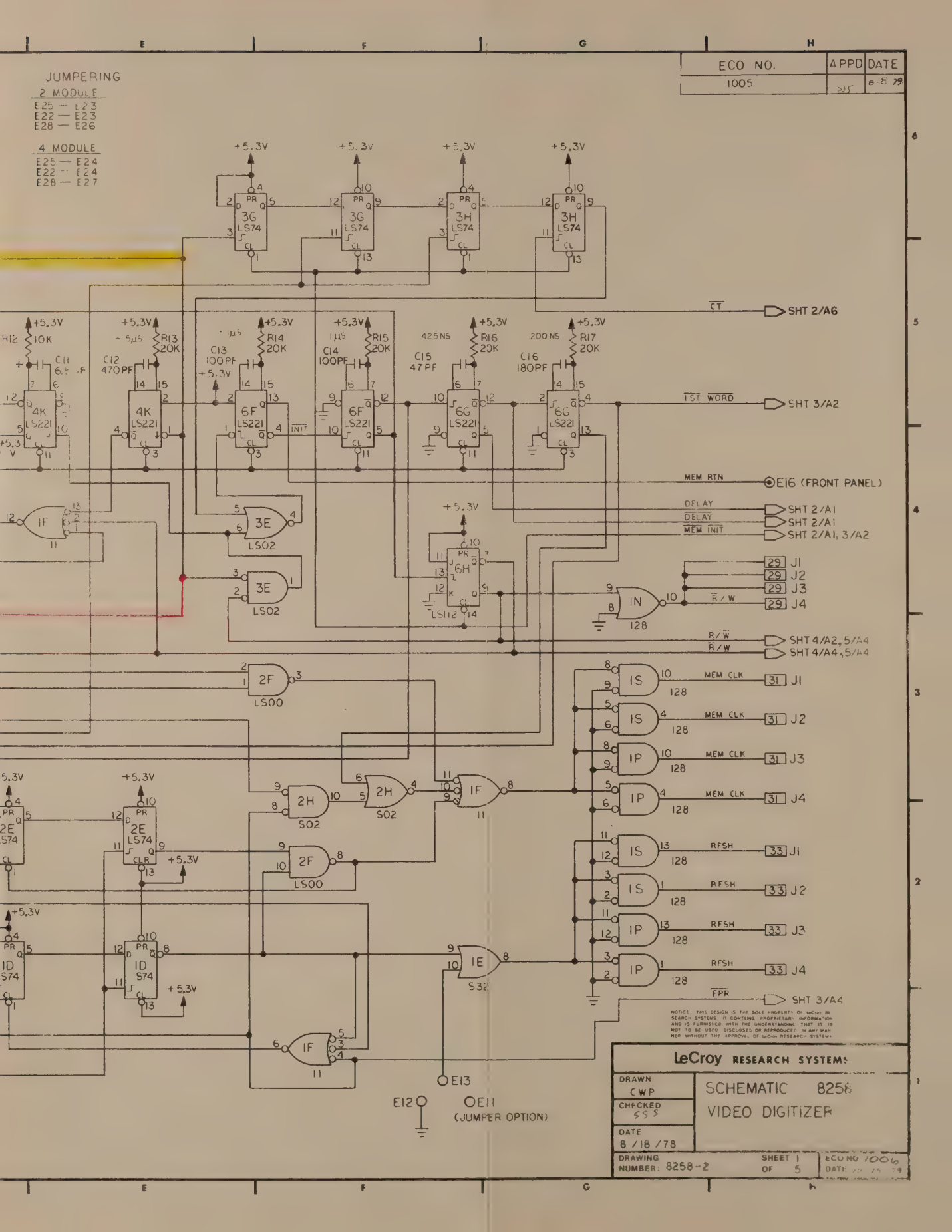
LeCroy RESEARCH SYSTEMS

DRAWN: S.MALM
CHECKED:
DATE: 6/6/77

WAVEFORM ANALYZER
MODEL 225G

DRAWING NUMBER: 225G-51
SHEET 6 OF 6
ECO NO. 554
DATE 6/30/77


+5.3V
E9
R7 150
CR3 "READ"
E10
2D
R8 150
E4
CR4 "READY"
E3
LS00
3B
R9 150
E5
CR5 "SAMPLING"
E6
J1 35 MEM RET
J6 19
SHT 3/A6 PLCK
J1 39 MEM EN
J2 39
J3 39
J4 39
IN 128
SHT 2/H6
E17
E18
E19
E20
E21
1B LS191
2C S112
1C LS74
E23
E27
E28
E26
E24
E22
E25
SHT 4/A2,5/A4 BL LOAD
SHT 2/A3 STROBE
SHT 3/A5,2/A6 RST
SHT 2/A5 STROBE
SHT 2/H2,3/A1 CREN
(FRONT PANEL) E7 ENABLE SAMPLING
(FRONT PANEL) E8 CLK
3D 265
R28 1K
R4 51
1E S32
J6 17 ADC CLK
R5 82
R6 510
5K 10124
-5.3V
SHT 4/A2,5/A4 SR LOAD
2H LS02
4G LS74
DISABLE RFSH
SHT 3/A5 RST
SHT 3/A4 ROD
+6V
F1 3A
L1
CR1 IN4139
C1 6.8V
C2, 21-43 47μF
C3 47μF
GND
C4 6.8V
C5 47μF
C6 47μF
-6V
F2 1A
L2
CR2 IN4005
-24V
6B 79MG
C7 6.8V
C8 6.8V
R1 20K
R2 22K
R3 20K
-12V
C9 .01μF
R10 620
1A LS13
~100KHZ
~2.5MHz
C10 510PF
R11 620


ECO NO. 1005
APPD
DATE 8-8-79
JUMPERING
2 MODULE
E25 — E23
E22 — E23
E28 — E26
4 MODULE
E25 — E24
E22 — E24
E28 — E27
+5.3V
3G LS74
3H LS74
RI2 10K
C11 6.8 PF
C12 470PF
RI3 20K
~5µS
C13 100PF
RI4 20K
~1µS
C14 100PF
RI5 20K
1µS
C15 47PF
RI6 20K
425NS
C16 180PF
RI7 20K
200NS
4K LS221
6F LS221
6G LS221
INIT
CT
SHT 2/A6
1ST WORD
SHT 3/A2
MEM RTN
E16 (FRONT PANEL)
DELAY
SHT 2/A1
MEM INIT
SHT 2/A1, 3/A2
1F
3E LS02
6H LS112
1N 128
29 J1
29 J2
29 J3
R/W
29 J4
SHT 4/A2, 5/A4
SHT 4/A4, 5/A4
2F LS00
1S 128
MEM CLK
31 J1
31 J2
1P 128
31 J3
31 J4
2H S02
2E LS74
1D S74
RFSH
33 J1
33 J2
33 J3
33 J4
1E S32
FPR
SHT 3/A4
E13
E12
E11
(JUMPER OPTION)
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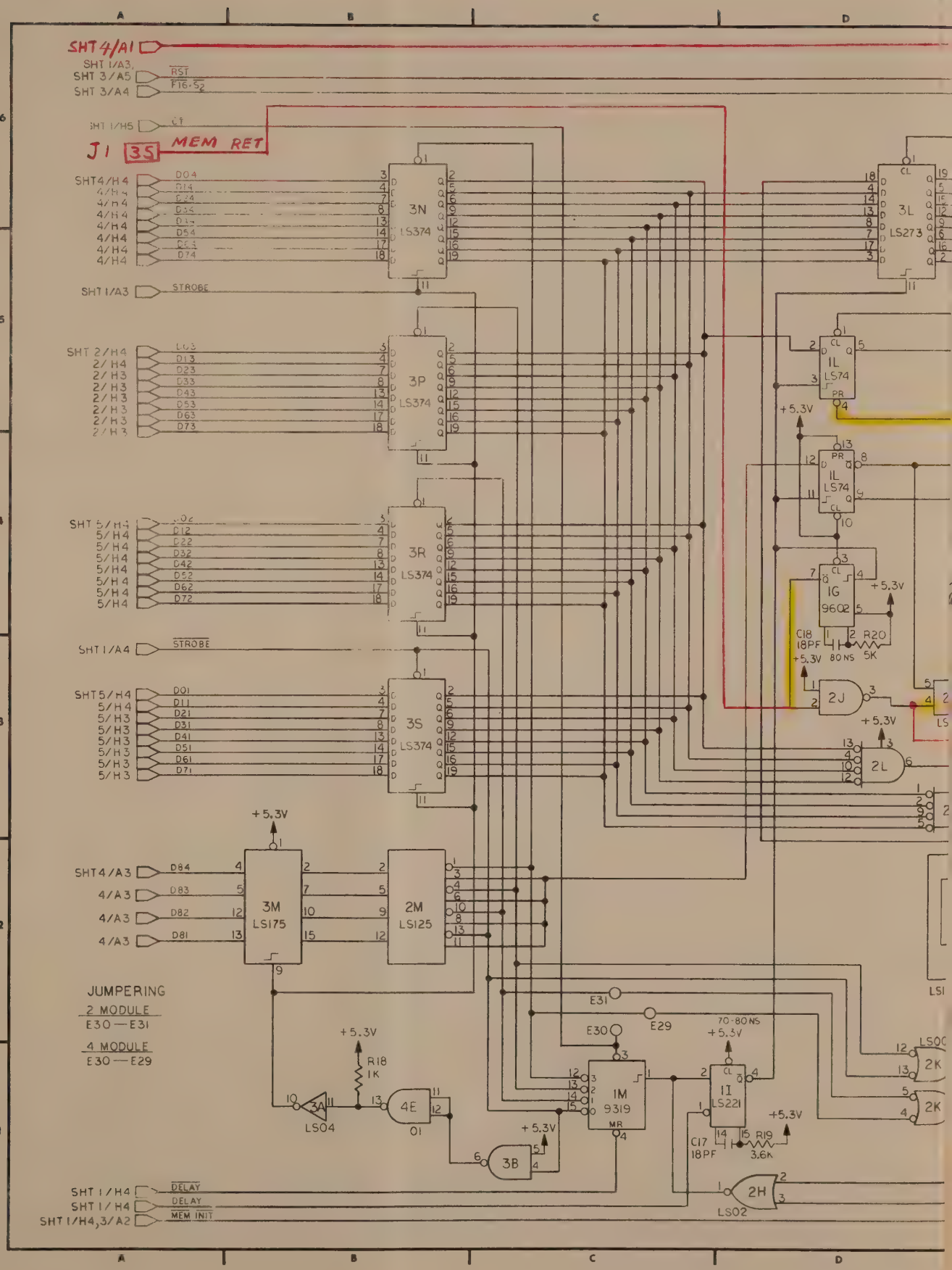
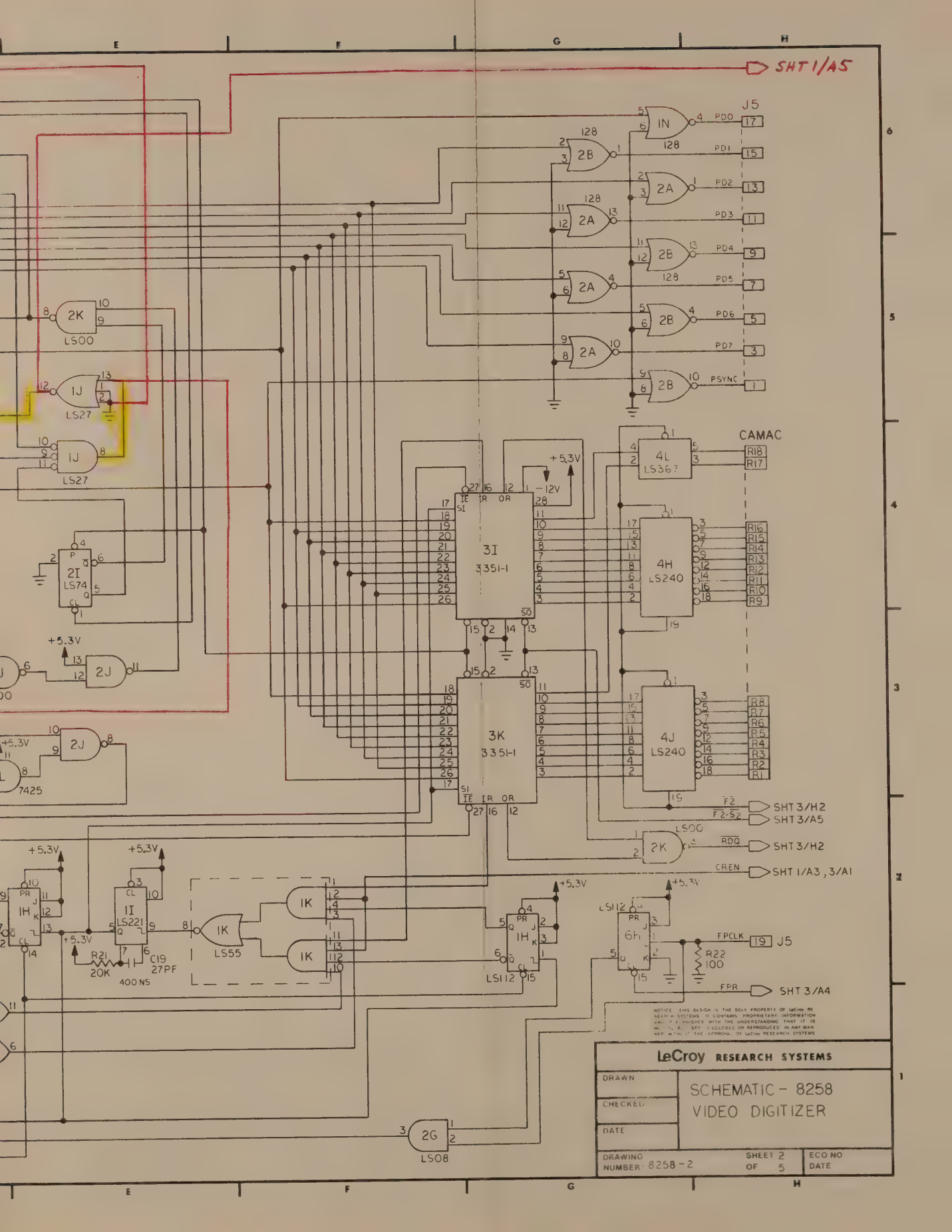
LeCroy RESEARCH SYSTEMS
DRAWN CWP
CHECKED SSS
DATE 8/18/78
SCHEMATIC 8258
VIDEO DIGITIZER
DRAWING NUMBER: 8258-2
SHEET 1 OF 5
ECO NO 1006
DATE


SHT 4/A1
SHT 1/A3,
SHT 3/A5
SHT 3/A4
RST
F16·S2
SHT 1/H5
CT
J1 35 MEM RET
SHT4/H4
4/H4
4/H4
4/H4
4/H4
4/H4
4/H4
4/H4
D04
D14
D24
D34
D44
D54
D64
D74
3N
LS374
SHT 1/A3
STROBE
3L
LS273
SHT 2/H4
2/H4
2/H3
2/H3
2/H3
2/H3
2/H3
2/H3
D03
D13
D23
D33
D43
D53
D63
D73
3P
LS374
1L
LS74
+5.3V
SHT 5/H4
5/H4
5/H4
5/H4
5/H4
5/H4
5/H4
5/H4
D02
D12
D22
D32
D42
D52
D62
D72
3R
LS374
1G
9602
C18
18PF
R20
5K
80 NS
SHT 1/A4
STROBE
SHT 5/H4
5/H4
5/H3
5/H3
5/H3
5/H3
5/H3
5/H3
D01
D11
D21
D31
D41
D51
D61
D71
3S
LS374
2J
2L
+5.3V
SHT4/A3
4/A3
4/A3
4/A3
D84
D83
D82
D81
3M
LS175
2M
LS125
JUMPERING
2 MODULE
E30 — E31
4 MODULE
E30 — E29
E31
E30
E29
70-80 NS
R18
1K
3A
LS04
4E
01
3B
1M
9319
MR
1I
LS221
C17
18PF
R19
3.6K
2H
LS02
2K
SHT 1/H4
SHT 1/H4
SHT 1/H4,3/A2
DELAY
DELAY
MEM INIT


SHT 1/A5
J5
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
PSYNC
CAMAC
+5.3V
-12V
3I
3351-1
3K
3351-1
4L
LS367
4H
LS240
4J
LS240
R18
R17
R16
R15
R14
R13
R12
R11
R10
R9
R8
R7
R6
R5
R4
R3
R2
R1
F2
F2·S2
SHT 3/H2
SHT 3/A5
LS00
RDQ
SHT 3/H2
CREN
SHT 1/A3, 3/A1
FPCLK
J5
R22
100
FPR
SHT 3/A4
2K
LS00
1J
LS27
2I
LS74
2J
7425
1H
1I
LS221
R21
20K
C19
27PF
400 NS
1K
LS55
LS112
2G
LS08
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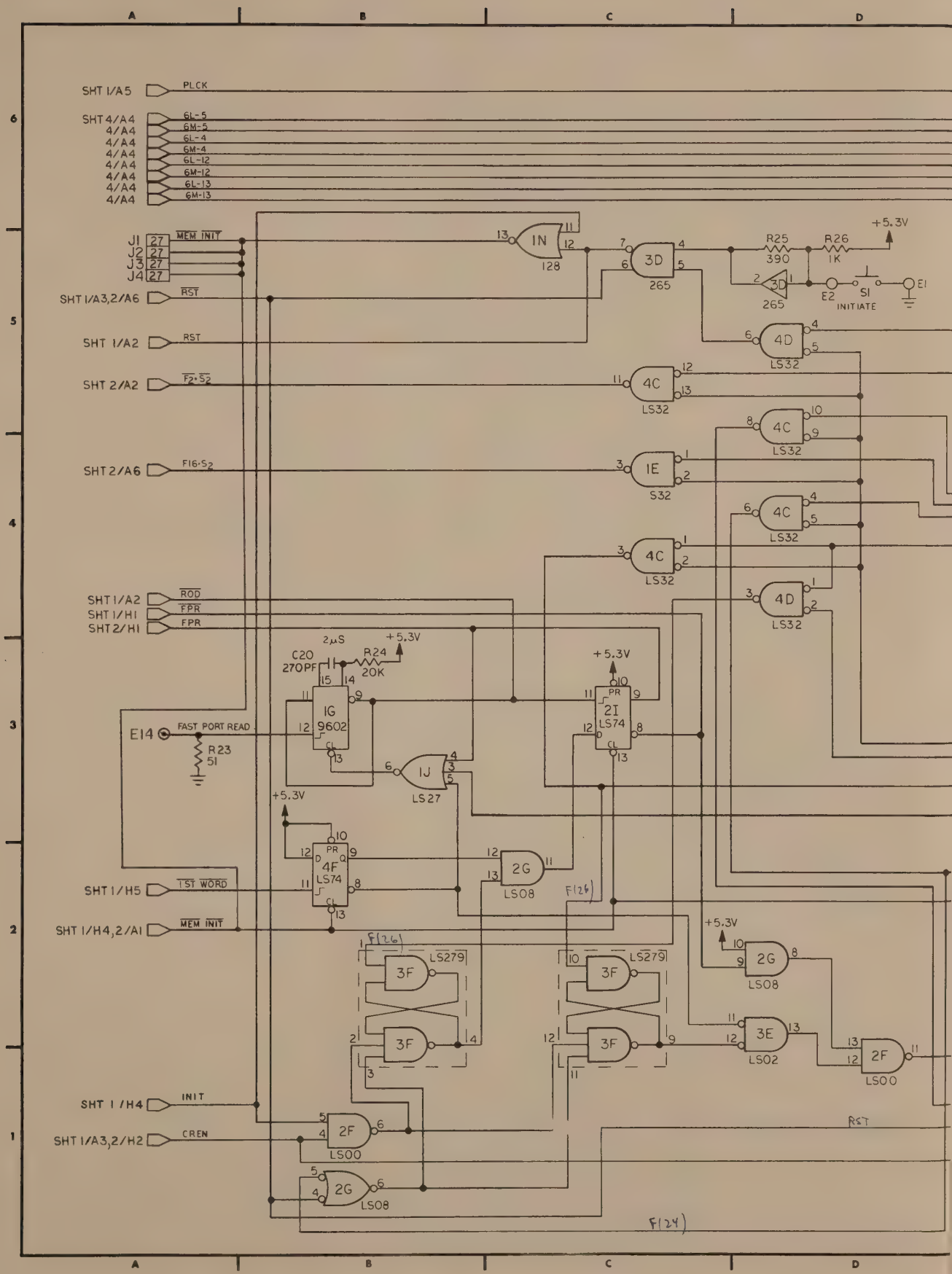
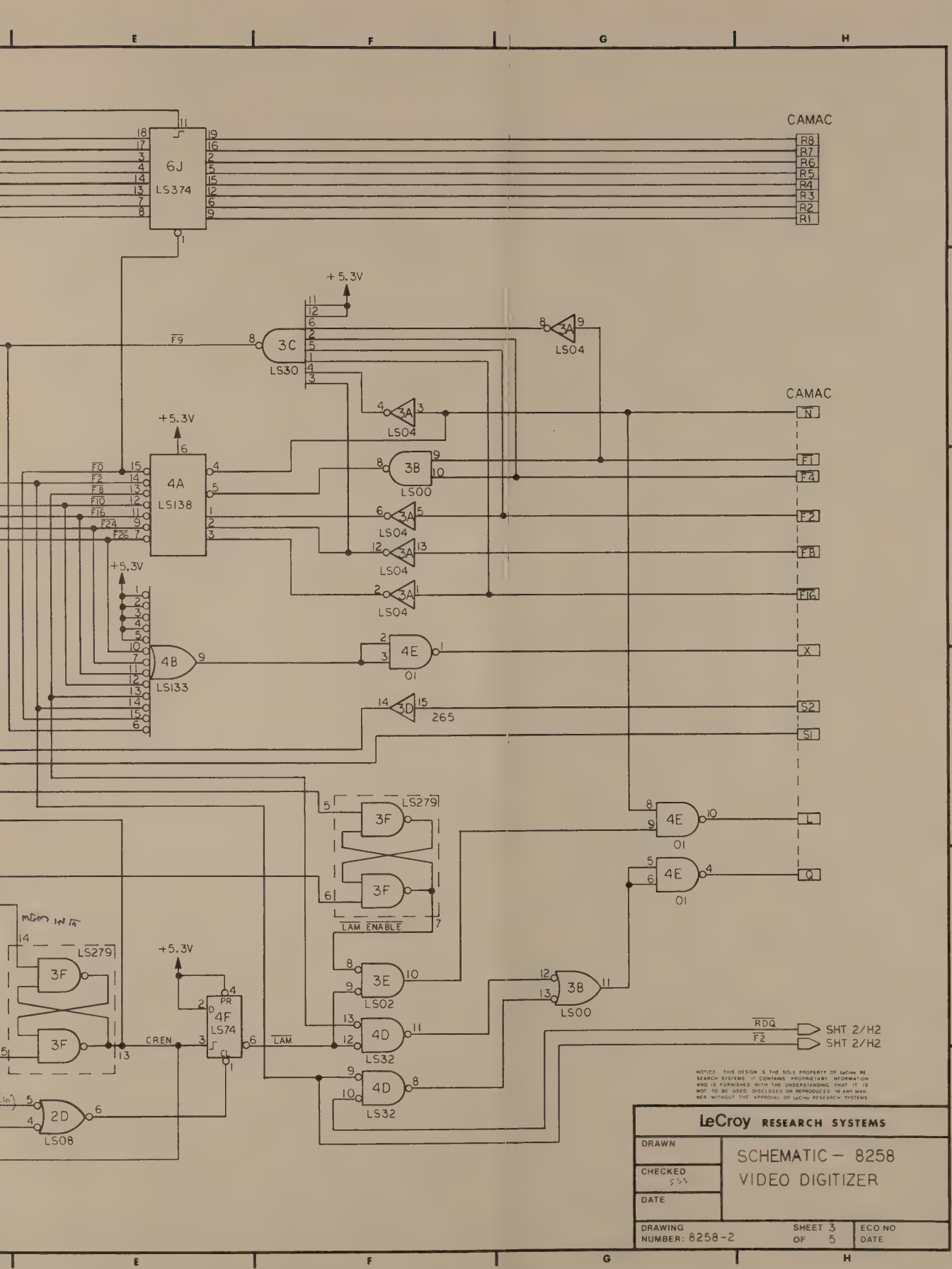
LeCroy RESEARCH SYSTEMS
DRAWN
CHECKED
DATE
SCHEMATIC - 8258
VIDEO DIGITIZER
DRAWING NUMBER 8258-2
SHEET 2 OF 5
ECO NO
DATE


SHT 1/A5 PLCK
SHT 4/A4 6L-5
4/A4 6M-5
4/A4 6L-4
4/A4 6M-4
4/A4 6L-12
4/A4 6M-12
4/A4 6L-13
4/A4 6M-13
J1 27 MEM INIT
J2 27
J3 27
J4 27
SHT 1/A3,2/A6 RST
SHT 1/A2 RST
SHT 2/A2 F2·S2
SHT 2/A6 F16·S2
SHT 1/A2 ROD
SHT 1/H1 FPR
SHT 2/H1 FPR
E14 FAST PORT READ
R23 51
SHT 1/H5 TST WORD
SHT 1/H4,2/A1 MEM INIT
SHT 1/H4 INIT
SHT 1/A3,2/H2 CREN
1N 128
3D 265
R25 390
R26 1K
+5.3V
E2
S1 INITIATE
E1
4D LS32
4C LS32
1E S32
C20 270PF
R24 20K
2μS
1G 9602
1J LS27
2I LS74
4F LS74
2G LS08
3F LS279
3E LS02
2F LS00
F(26)
F(24)
RST



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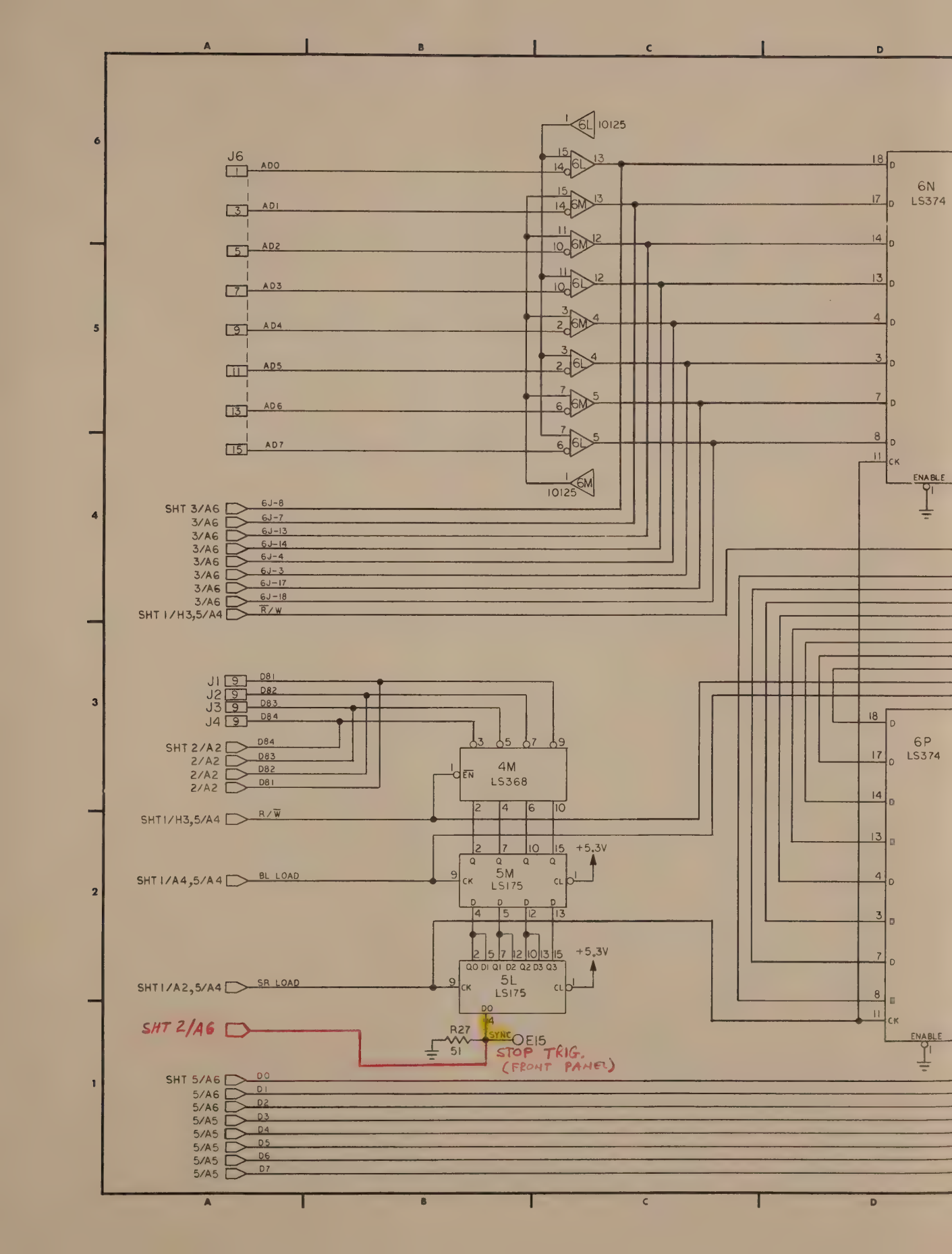
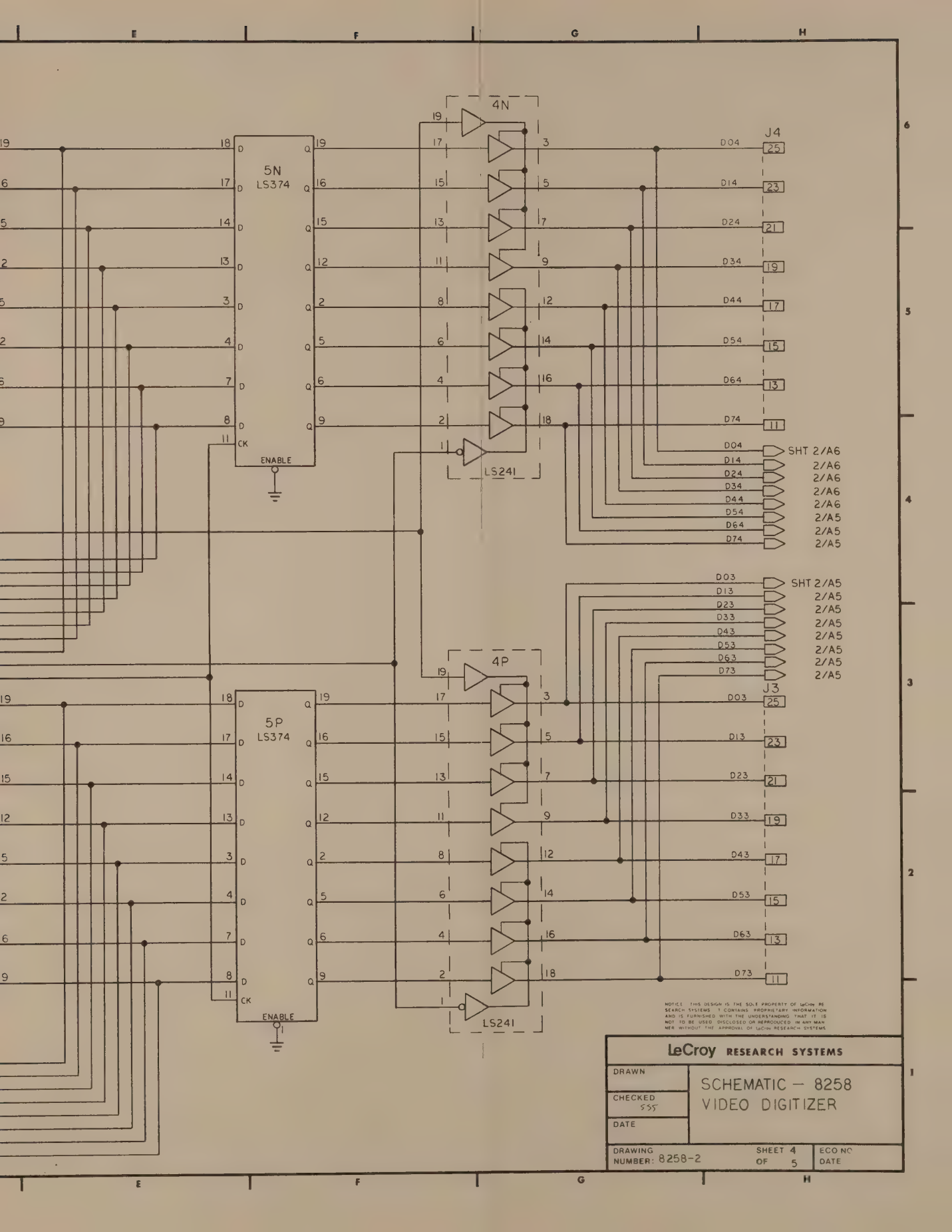
LeCroy RESEARCH SYSTEMS

DRAWN	SCHEMATIC – 8258 VIDEO DIGITIZER
CHECKED SSS	
DATE	
DRAWING NUMBER: 8258-2	SHEET 3 OF 5
ECO NO DATE	


J6
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
6L 10125
6M 10125
6N LS374
6P LS374
ENABLE
SHT 3/A6
3/A6
3/A6
3/A6
3/A6
3/A6
3/A6
3/A6
SHT 1/H3,5/A4
6J-8
6J-7
6J-13
6J-14
6J-4
6J-3
6J-17
6J-18
R/W
J1 D81
J2 D82
J3 D83
J4 D84
SHT 2/A2
2/A2
2/A2
2/A2
4M LS368
SHT1/H3,5/A4
SHT1/A4,5/A4
BL LOAD
5M LS175
+5.3V
SHT1/A2,5/A4
SR LOAD
5L LS175
SHT 2/A6
R27
51
SYNC
E15
STOP TRIG. (FRONT PANEL)
SHT 5/A6
5/A6
5/A6
5/A5
5/A5
5/A5
5/A5
5/A5
D0
D1
D2
D3
D4
D5
D6
D7


E
F
G
H
6
5
4
3
2
1
4N
5N
LS374
ENABLE
LS241
J4
D04
D14
D24
D34
D44
D54
D64
D74
SHT 2/A6
2/A6
2/A5
4P
5P
J3
D03
D13
D23
D33
D43
D53
D63
D73
SHT 2/A5
2/A5
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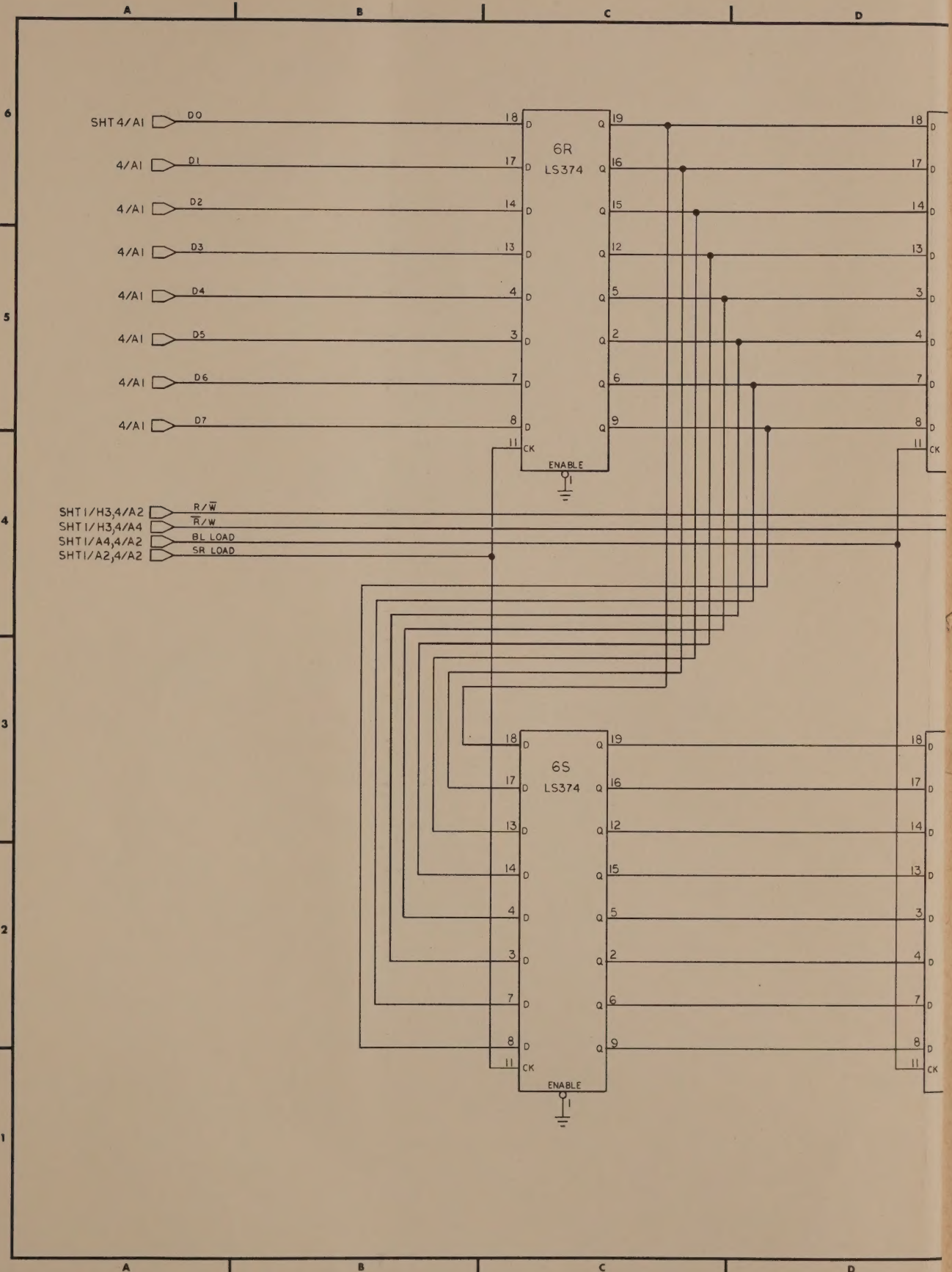
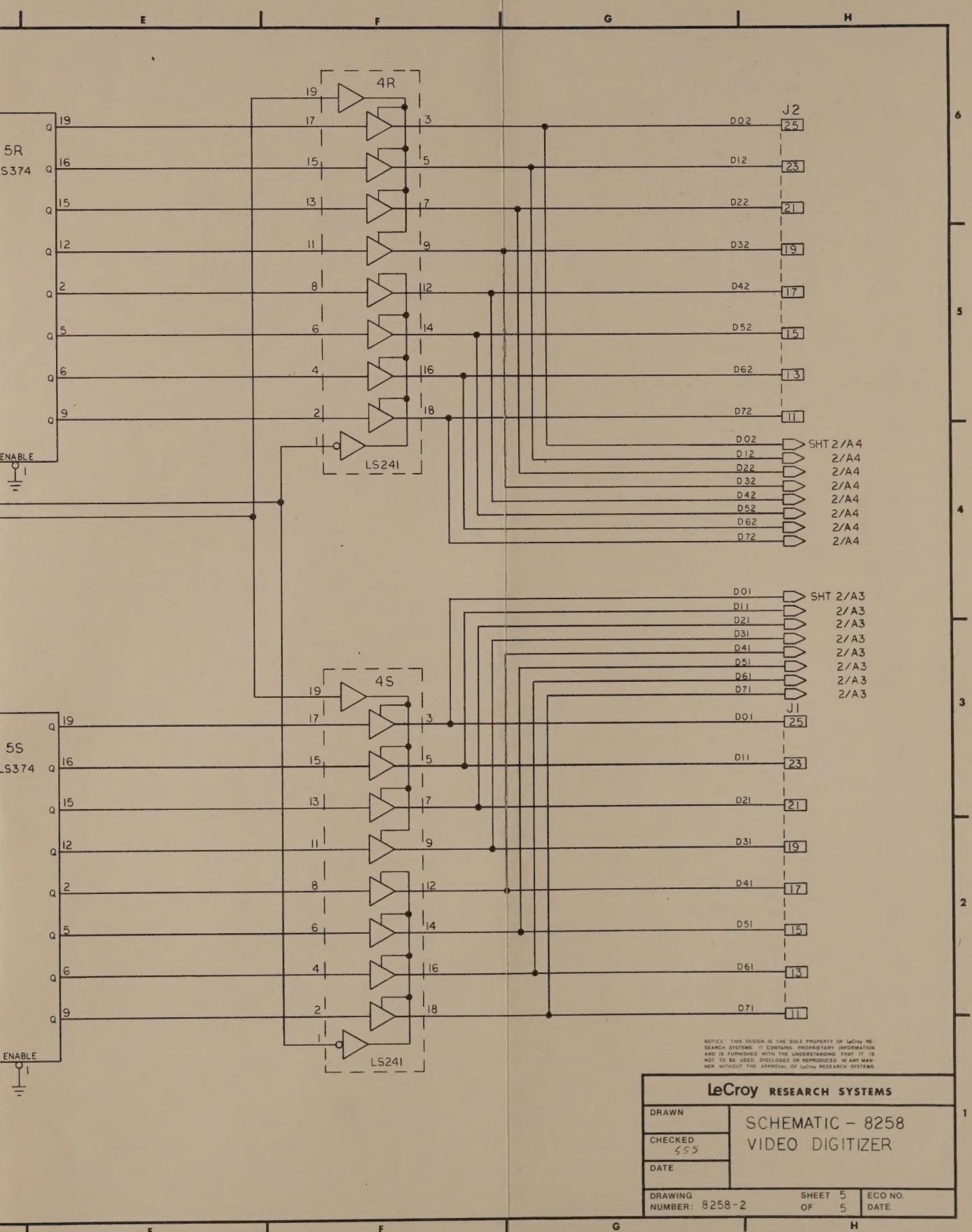
LeCroy RESEARCH SYSTEMS
DRAWN
CHECKED
555
DATE
SCHEMATIC – 8258
VIDEO DIGITIZER
DRAWING NUMBER: 8258-2
SHEET 4 OF 5
ECO NO
DATE


A
B
C
D
6
5
4
3
2
1
SHT4/A1
4/A1
4/A1
4/A1
4/A1
4/A1
4/A1
4/A1
D0
D1
D2
D3
D4
D5
D6
D7
6R
LS374
ENABLE
SHT1/H3,4/A2
SHT1/H3,4/A4
SHT1/A4,4/A2
SHT1/A2,4/A2
R/W
R/W
BL LOAD
SR LOAD
6S
LS374
ENABLE
CK



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